## AMENDMENTS TO THE CLAIMS

Please amend claim 14 as set forth below:

1. (original) A digital signal processor, comprising:

a content addressable memory (CAM) array having a plurality of rows of CAM cells;

an array of storage elements having a plurality of rows of the storage elements coupled to the CAM array, each row of storage elements to store a number corresponding to a data word stored in one of the rows of the CAM cells; and

priority logic coupled to the array of storage elements, the priority logic to provide to a plurality of priority signal lines an indication of a location of a particular number in the array of storage elements, wherein the priority logic comprises:

a first plurality of compare circuits, each compare circuit coupled to one of the storage elements in the array of storage elements, and each compare circuit having a first input coupled to a storage element, a second input coupled to a match line, and an input/output line coupled to one of the plurality of priority signal lines; and

a delay circuit coupled to each of the first plurality of compare circuits.

2. (original) The digital signal processor of claim 1, wherein the delay circuit comprises a multiple tap delay circuit.

3. (original) The digital signal processor of claim 1, wherein the delay circuit comprises a plurality of delay elements, each of the plurality of delay elements coupled to one of the plurality of compare circuits.

4. (original) The digital signal processor of claim 3, wherein each of the delay elements is programmable.

5. (original) The digital signal processor of claim 1, wherein each of the compare circuits comprise a first transistor having a drain coupled to a corresponding priority

signal line and having a gate coupled to a corresponding storage element.

6. (original) The digital signal processor of claim 5, wherein the gate of the first transistor is coupled to the delay circuit through one or more logic gates.

7. (original) The digital signal processor of claim 6, wherein the delay circuit comprises a plurality of delay elements, each of the plurality of delay elements having an output coupled to one of the plurality of compare circuits.

8. (original) The digital signal processor of claim 7, wherein the one or more logic gates comprise a NAND gate having a first input coupled to a corresponding match line and a having a second input coupled to a corresponding output of one of the delay elements.

9. (original) The digital signal processor of claim 8, wherein the NAND gate has an output and wherein the one or more logic gates further comprise a NOR gate having a first input coupled the output of the NAND gate, and wherein the NOR gate has an output coupled to the gate of the first transistor.

10. (original) The digital signal processor of claim 1, further comprising:

a policy statement table for storing a plurality of policy statements; and

a priority index table for storing a plurality of priority numbers, each priority number associated with a corresponding policy statement and indicating the priority of the corresponding policy statement relative to the other policy statements, wherein the priority index table comprises the priority logic coupled to the policy statement table, wherein the priority logic provides the most significant priority number to a plurality of priority signal lines.

11. (original) The digital signal processor of claim 1, wherein the first plurality of compare circuits are coupled in a sequence, each of compare circuit having a third input coupled to a preceding compare circuit in the sequence.

12. (original) The digital signal processor of claim 11, wherein each of the compare circuits comprise a first transistor having a drain coupled to a corresponding priority signal line and having a gate coupled to a corresponding storage element, wherein the gate of the first transistor is coupled to the delay circuit through one or more logic gates.

13. (original) The digital signal processor of claim 12, wherein the third input of the compare circuit is coupled to the one or more logic gates.

14. (currently amended) The digital signal processor of claim 13, wherein the one or more logic gates comprise a first NOR gate having a first input ~~coupled the third~~ coupled to the third input of the compare circuit, the first NOR gate having an output coupled to the gate of the first transistor.

15. (original) The digital signal processor of claim 14, wherein each of the compare circuits further comprises a second NOR gate having an input coupled to the gate of the first transistor, the second NOR gate having an output coupled to the first NOR gate of a succeeding compare circuit in the sequence.

16. (previously presented) A method of operating a digital signal processor, comprising:

outputting a first priority number signal on a priority line coupled to a first column of compare circuits, the first priority number signal having one of at least two logical signal levels based, at least in part, on a comparison of priority number bits stored within a first column of priority number storage elements coupled to the first column of compare circuits; and

concurrently de-asserting a match line in the first column of compare circuits and outputting a second priority number signal on a next priority line coupled to a second column of compare circuits, the second priority number signal having one of the at least two logical signal levels based, in part, on a comparison of priority number bits stored within a second column of priority number storage elements coupled to the second column of compare circuits.

17. (original) The method of claim 16, further comprising de-asserting a match line in the second column of compare circuits.

18. (previously presented) A digital signal processor, comprising:

means for outputting a first priority number signal on a priority line coupled to a first column of compare circuits, the first priority number signal having one of at least two logical signal levels based, at least in part, on a comparison of priority number bits stored within a first column of priority number storage elements coupled to the first column of compare circuits; and

means for concurrently de-asserting a match line in the first column of compare circuits and outputting a second priority number signal on a next priority line coupled to a second column of compare circuits, the second priority number signal having one of the at least two logical signal levels based, in part, on a comparison of priority number bits stored within a second column of priority number storage elements coupled to the second column of compare circuits.

19. (original) The digital signal processor of claim 17, further comprising means for de-asserting a match line in the second column of compare circuits.